Cu CMP Barrier Slurry Development to Achieve Adjustable Rates and Selectivities for Capped and Un-Capped Cu/Low-K

Qianqiu (Christine) Ye, Matthew VanHanehem Ray Lavoie, John Quanci
Rodel, Inc.
Key Drivers for New Cu CMP Barrier Slurries

- Industry shifted from Al To Cu and is transferring from TEOS to low K material
  - Many potential integration schemes including use of capping layers
  - May require specific selectivity to Copper: Barrier: Dielectric: Caps

- Current and future ICs employ > 6 metal levels requiring high degree of planarization and topography correction.

- Barrier Slurry needs to balance the removal rates of various films to achieve the selectivities for the desired topography, planarization and dielectric loss targets
  - Tunable selectivity barrier slurries will be needed for all layers to satisfy many different integration schemes and goals
### Integration Architectures

<table>
<thead>
<tr>
<th>Integration Scheme</th>
<th>Low-k (90nm)</th>
<th>ULK (65nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>No Cap</strong></td>
<td><img src="image" alt="Diagram" /></td>
<td>N/A</td>
</tr>
<tr>
<td><strong>Single Cap</strong></td>
<td><img src="image" alt="Diagram" /></td>
<td><img src="image" alt="Diagram" /></td>
</tr>
<tr>
<td>Cap: SiO₂, a-SiCH, Si₃N₄, SiON, SiOC</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Dual-Cap</strong></td>
<td><img src="image" alt="Diagram" /></td>
<td><img src="image" alt="Diagram" /></td>
</tr>
<tr>
<td>Cap #1 / Cap #2: SiO₂ / a-SiC, Si₃N₄ / SiO₂</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Many potential integration schemes with different objectives will require different barrier slurry selectivities

<table>
<thead>
<tr>
<th>Capping</th>
<th>Stack</th>
<th>Integration requirement</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncapped</td>
<td>CDO/TaN/Cu</td>
<td>1. Polish CDO</td>
<td>Planarize CDO</td>
</tr>
<tr>
<td>Uncapped</td>
<td>CDO/TaN/Cu</td>
<td>2. Stop on CDO</td>
<td>No planarization or topography correction</td>
</tr>
<tr>
<td>Single Cap</td>
<td>CDO/Cap/TaN/Cu</td>
<td>3. Stop on Cap</td>
<td>No planarization or topo correction</td>
</tr>
<tr>
<td>Single Cap</td>
<td>CDO/Cap/TaN/Cu</td>
<td>4. Remove Cap and polish CDO</td>
<td>- Planarize CDO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5. Thin/Planarize Cap</td>
<td>- Planarize Cap</td>
</tr>
<tr>
<td>Dual Cap</td>
<td>CDO/Cap 2/Cap 1/TaN/Cu</td>
<td>6. Remove Caps &amp; polish CDO</td>
<td>Planarize CDO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7. Remove top Cap 1 and Thin Bottom Cap 2</td>
<td></td>
</tr>
<tr>
<td>Dual Cap</td>
<td>CDO/Cap 2/Cap 1/TaN/Cu</td>
<td>8. Remove top Cap 1 and Stop on bottom Cap 2</td>
<td>No planarization or topography correction</td>
</tr>
</tbody>
</table>
Objective: Meet varying customer integration and performance requirements with a tunable selectivity family of barrier slurries for uncapped and capped Low K applications.

- Composition that permits adjustment of selectivities to suit specific integration targets by simple changes in the concentration of components.

Outcome: A family of Cu CMP barrier slurries was developed based on combined blanket removal rate and pattern topography models for the Politex and IC pads.

- All slurry components and their interaction/impact on copper, ILD, capping materials and barrier removal rates have been modeled.
- Several formulations were chosen to confirm the models as well as generate pattern wafer data
- Models allow rapid formulation customization to meet customer requirements
Blanket Removal Rate Model Example

- 5+ parameters can be adjusted to meet desired removal rates (2 shown)
- White area indicates design space for desired removal rates
- Design space shown optimized around LK barrier slurry family (example)
- Response surfaces created for both IC1010 and Politex pads

Blacket Removal Rate Response Surface with CDO wafers

Intersection of 3 desired RR’s
## Barrier/Low-k Slurry Recommendations

<table>
<thead>
<tr>
<th>Slurry</th>
<th>Ta RR (Å/min)</th>
<th>TaN RR (Å/min)</th>
<th>TEOS RR (Å/min)</th>
<th>Cu RR (Å/min)</th>
<th>CORAL RR (Å/min)</th>
<th>Si₃N₄ RR (Å/min)</th>
<th>a-SiCH RR (Å/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK-309</td>
<td>468</td>
<td>1025</td>
<td>489</td>
<td>214</td>
<td>~0</td>
<td>267</td>
<td>30</td>
</tr>
<tr>
<td>LK-301</td>
<td>562</td>
<td>1030</td>
<td>707</td>
<td>125</td>
<td>109</td>
<td>365</td>
<td>124</td>
</tr>
<tr>
<td>LK-310</td>
<td>1300-1500</td>
<td>1338</td>
<td>815</td>
<td>48</td>
<td>771</td>
<td>380</td>
<td>877</td>
</tr>
</tbody>
</table>

**IC1010 Pad**

- **High rate slurry recommended for uncapped topography correction**
- **Slurry recommended for dual-top hard-mask scheme (remove top HM and maintain bottom HM)**
- **Slurry recommended for minimal Low-k or cap removal (i.e., no HM or single-top HM)**

<table>
<thead>
<tr>
<th>Slurry</th>
<th>Ta RR (Å/min)</th>
<th>TaN RR (Å/min)</th>
<th>TEOS RR (Å/min)</th>
<th>Cu RR (Å/min)</th>
<th>CORAL RR (Å/min)</th>
<th>Si₃N₄ RR (Å/min)</th>
<th>a-SiCH RR (Å/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK-309</td>
<td>319</td>
<td>708</td>
<td>499</td>
<td>243</td>
<td>189</td>
<td>237</td>
<td>256</td>
</tr>
<tr>
<td>LK-301</td>
<td>434</td>
<td>866</td>
<td>752</td>
<td>433</td>
<td>663</td>
<td>333</td>
<td>666</td>
</tr>
<tr>
<td>LK310</td>
<td>1300-1500</td>
<td>1282</td>
<td>810</td>
<td>408</td>
<td>978</td>
<td>380</td>
<td>879</td>
</tr>
</tbody>
</table>

**Notes:**
- Wafers processed at 2psi down force, 120rpm platen speed, 114rpm carrier speed
- Polishing tool: AMAT MIRRA polisher

RODEL, INC. – 10/02
Selective LK film removal

- Selectivity to low K and capping materials achieved by addition of component A
- Optimization of slurry formula using all slurry components allows tunability

### Removal Rates & Selectivities

![Graph showing removal rates and selectivities](image-url)
LK300 Family of Barrier Slurries

- LK300 family of barrier slurries developed using slurry models and understanding of customer performance requirements.
  - High barrier removal rate slurries developed based on TEOS/CDO/Cap selectivity requirements
  - LK-309: high selectivity, maintains topography after barrier clear and allows long over polishing with no ILD loss.
  - LK-301: medium selectivity, corrects topography after barrier clear during over polishing with minimized ILD loss.
  - LK-310: low/non-selective, increased topography correction at the expense of ILD loss.
- Multiple slurries within slurry family allows flexibility to meet the requirements of customer specific integration schemes.
  - LK301, 309 and 310 are in development phase.
  - LK-300 slurry family extendable to capped low-k architectures
Uncapped Patterned Low-k wafers polished

854LKC001 (No Hardmask)

0.25um trenches etched through 100A Ta, 4K CORAL, stop on 500A SiCN over 5.5K thermal oxide, Si.
250 Ta / 1K Cu seed, 10K CuE (annealed).
Good topography performance achieved with the High-Selectivity Barrier Slurries on CDO Pattern Wafers

- Dishing is less than 350Å after ~350Å Ta clear
- Long over polishing window (+60s) with little further ILD loss

First Step Cu Polish

Platen 1 – EPL2360  
100um Lines ≅ 760Å

Platen 2 – RLS3126  
50um Lines ≅ 650Å

Dishing and Erosion

Over-Polish Time (s)

Field Dielectric Loss

100 um
50 um
70% (7_3)
ILD Loss
90% (9_1)
Excellent topography performance achieved with the Medium-Selectivity Barrier Slurries on CDO Pattern Wafers

- Dishing are less than 400Å after ~400Å Ta clear
- Long over polishing window (+60s) with minimized ILD loss

**First Step Cu Polish**

- Platen 1 – EPL2360
  - 100um Lines = 760Å
- Platen 2 – RLS3126
  - 50um Lines = 650Å
**Excellent topography performance achieved with the **Low-selectivity** Barrier Slurries on CDO Pattern Wafers**

- Dishing are less than 200Å after ~400Å Ta clear
- Topography correction achieved during over-polish with ILD loss.

**First Step Cu Polish**

- Platen 1 – EPL2360
  - 100μm Lines = 760Å
- Platen 2 – RLS3126
  - 50μm Lines = 650Å
A family of low K barrier removal slurries has been developed with the following features:

- Tunability of the relative removal rates of Cu, dielectric materials and caps allows optimization of final wafer topography and dielectric/metal loss for specific customer integration scheme
- High barrier removal rates provide high throughput
- Significant reduction in topography can be achieved during the barrier removal step without compromising dielectric loss
- Formulations afford low defectivity and excellent surface quality
- Slurry component interactions are fully modeled to allow Rodel to predict the best slurry to meet a given set of performance requirements
- Selectivity on TEOS/SiC and TEOS/CDO allows the slurry family to be employed for both Low K capped and uncapped patterned wafer polishing
Contacts

Christine Ye, Scientist
John Quanci, R&D Manager
Matthew VanHanehem, Integration Engineer
Kelly Block, Product Manager
Rodel, Inc.