Consumable Technologies to Cover a Wide Variety of CMP Applications

US CMPUG, 9 April 2008
Presenter: Paul Feeney, CMP Fellow
Outline

- Need for new IC CMP applications

- Existing applications
  - Tungsten, Dielectric, Copper, Barrier

- New applications
  - Emerging IC applications
  - Extension beyond IC’s

- Summary
Why Do We Need New CMP Applications?

- New CMP applications arise when continuous improvement of consumables and equipment are not sufficient
- New applications are driven by smaller dimensions
  - Requirements for a given CMP process get tougher
    - Step function in performance needed
    - Need to optimize away from general purpose consumables
  - IC integration changes with each new advanced node
    - New and more complex structures drive new combinations of existing materials
    - Increased complexity leads to segmentation of requirements
    - New materials required to get chip performance and yield
  - Benefits of CMP spilled over into DRAM and NVRAM/flash
    - Accelerated by performance requirements and falling CMP CoO
# ITRS 2007 Planarization Applications

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<tr>
<td>DRAM 1/2 Pitch</td>
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<td>57nm</td>
<td>50nm</td>
<td>45nm</td>
<td>40nm</td>
<td>35nm</td>
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## Major Applications

### Dielectrics
- Shallow trench isolation (STI) [direct]
- Premetal dielectric (PMD) [target & selective]
- Interlevel dielectric (ILD) [memory]
- New applications [i.e. Si nitride]

### Conductors
- Polysilicon & target [selective]
- Tungsten/buffer [contact & via]
- Copper/barrier [4.0 > κ eff > 2.5]
- Copper/new barrier [2.7 > κ eff > 2.0]
- Copper/new barrier [2.2 > κ eff > 1.4]
- New applications [i.e. new contact]

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

- **Research Required**
- **Development Underway**
- **Qualification / Pre-Production**
- **Continuous Improvement**

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## ITRS 2007 Planarization Consumables

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<td>High solids slurries</td>
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<td>Slurries with low solids/defects/cost</td>
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<td>Optimized formulations from tunable platforms</td>
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<td>Fluids for chemical enhanced planarization and ECMP</td>
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<td>Cleaning and buff solutions tailored to applications</td>
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<td>Urethane pads for new applications</td>
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<td>Abrasive containing pads</td>
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<td>Range of alternative pads for planarity/defects/cost</td>
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- Research Required
- Development Underway
- Qualification / Pre-Production
- Continuous Improvement
## Core Product Pipeline
Advanced Solutions Across Applications

<table>
<thead>
<tr>
<th>Tungsten</th>
<th>Advanced Dielectric / ILD</th>
<th>Copper</th>
<th>Barrier</th>
<th>CMP Pads</th>
<th>Emerging Materials</th>
</tr>
</thead>
<tbody>
<tr>
<td>W2000 Series</td>
<td>Semi-Sperse Series</td>
<td>C5000 Series</td>
<td>B5200 Series</td>
<td>D100</td>
<td>Aluminum</td>
</tr>
<tr>
<td>W6000 Series</td>
<td>D1300 Series</td>
<td>C6000 Series</td>
<td>B6618</td>
<td></td>
<td>Ruthenium</td>
</tr>
<tr>
<td>W7000 Series</td>
<td>D3500/D4500 Series</td>
<td>C7000 Series</td>
<td>B7000 Series</td>
<td></td>
<td>Nitride</td>
</tr>
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<td></td>
<td>D6700 Series</td>
<td>C8000 Series</td>
<td>B8500 Series</td>
<td></td>
<td>Dielectric Poly</td>
</tr>
<tr>
<td></td>
<td>D8100 Series</td>
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<td></td>
<td>Noble Metals Metal Gates</td>
</tr>
</tbody>
</table>

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## Tungsten Solutions for Advanced Technologies

### Selective Approach

**W7000**

<table>
<thead>
<tr>
<th>Customer Requirements</th>
<th>High Selective Solution for Advanced Technologies</th>
</tr>
</thead>
<tbody>
<tr>
<td>Formulation</td>
<td>Fumed Silica and Etch Inhibitors</td>
</tr>
<tr>
<td>Performance</td>
<td>W:Ox (200:1) Erosion &lt; 200Å Defectivity = &lt; 0.25X</td>
</tr>
<tr>
<td>Manufacturing Status</td>
<td>Commercial in Japan</td>
</tr>
</tbody>
</table>

### Tunable Selectivity Approach

**W7300**

<table>
<thead>
<tr>
<th>Customer Requirements</th>
<th>Tunable Selectivity for Advanced Technologies</th>
</tr>
</thead>
<tbody>
<tr>
<td>Formulation</td>
<td>Colloidal Silica and Etch Inhibitors, Compatible with All Other CMC W Products</td>
</tr>
<tr>
<td>Performance</td>
<td>W:Ox (Tunable) Erosion &lt; 200Å Defectivity = &lt; 0.25X</td>
</tr>
<tr>
<td>Manufacturing Status</td>
<td>Commercial in Japan</td>
</tr>
</tbody>
</table>
Edge-Over-Erosion (EOE) Performance

EOE is significantly reduced / eliminated with our advanced WIN™ products
Best-in-Class Defect Performance

Normalized Counts

Spots on Dielectric  Spots on Metal  Scratches

W2000  W7000  W7300

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W7300 Best-in-Class Performance *Buff Step*

1st Step: W2000 1:1 dil

Plug Device
0.16 um/25% density

Erosion (Å)

Significant reduction in both defectivity and erosion after W7300 buff step
**WIN™ W7300 B21 / Epic® D100 Combo**

*Erosion Performance – Mirra 200mm*

**WBAApps117: Patterned Plug Oxide Erosion**
D100 vs IC1000 for WIN™ W7300-B21 on Ebara

- **200 nm Via, 25% pattern density**

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**Polish Process**
- BSP = 225 hPa
- SCP = 275 hPa
- RRP = 225 hPa
- CS = 55 rpm
- SFR = 150 ml/min
- Polish time = 60 s

**IC1000 Pad**
- PS (IC1000) = 100 rpm

**D100 Pad**
- PS (D100) = 125 rpm

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D100 Improved Defectivity

Defect and Scratch Counts
(MIT 854 Mask Patterned Wafers)

Total Defects

Average Scratch Count
18

Average Scratch Count
28

D100
Pad
Con. hard pad

> 35% defectivity reduction by using D100 pads

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D100 Longer Pad Life

- Longer pad life confirmed in high volume manufacturing
  - 2.5x conventional hard pad
  - 4x polyurethane impregnated polyester pad

- Improved CoO for Customers

** 15 mils groove depth
iDIEL™ D6720

and Extension to STI Applications

Abrasive Type

Chemistry

Hydrothermal Ceria

pH ~ 5.1
High Purity (no KOH)
Rate Control Additive

Self-Stopping Additive (SSA)

Mechanism

Balanced Chemical & Mechanical
high Ox/SiN selectivity

Self-Stopping When Added to C2

Mean Particle Size

~ 90 nm

none

Particle Concentration (POU)

< 1.0%

none

Method of Use

2X Concentrated
POU or In-line mixing
with B10 or by itself

POU Mixing
With D6720

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iDIEL™ D6720

Dielectric Removal on ILD Pattern

Planarity Target (SH + ~1500A)

D6720 planarizes faster compared to SS25E (polishing time can be shorter)
iDIEL™ D6720

D6720 shows 3X reduction in defectivity compared to SS25E
iDIEL™ D6720

POU Mixing of SSA - ILD Test Pattern

POU addition of SSA (B10) to D6720 reduces WID variation >3X
POU Mixing of SSA - STI Test Pattern (Logic)

D8100 is better than D6720 for planarity on STI test pattern

Range ~ 400A

Range ~ 790A

D6720+B10 (135:65) = 90 sec

D8100-A10+B10 (135:65) = 90 sec
D8100 is better than competitor slurry for planarity on STI test pattern
Formulation Design for C8100

- pH buffered near neutral to balance oxidation/dissolution mechanisms
- Addition of “dual functional” additive for Cu surface passivation

NFFC = “Novel Film Formation Chemistry”
## C8100 Slurry Properties

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>C8100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dilution Ratio</td>
<td>5X – 10X</td>
</tr>
<tr>
<td>pH (at POU)</td>
<td>6</td>
</tr>
<tr>
<td>Particle</td>
<td>Nano-Colloidal Silica</td>
</tr>
<tr>
<td>Particle % (at POU)</td>
<td>0.5 – 1.0%</td>
</tr>
<tr>
<td>Peroxide Addition</td>
<td>1%</td>
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</tbody>
</table>

## C8100 Selectivity

<table>
<thead>
<tr>
<th>Downforce (psi)</th>
<th>Copper Removal Rate (Ang/min)</th>
<th>Tantalum Removal Rate (Ang/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>2420</td>
<td>0</td>
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<tr>
<td>1.0</td>
<td>4360</td>
<td>0</td>
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</tbody>
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Polishing Tool Fault Simulation – iCue® C8100

C8100 - Copper Blanket Defect Pareto vs Tool Hang-up Time

300mm AMAT Reflexion

No Corrosion

Note: SP1 Copper Defect Threshold @ 0.25μm
D100 Enhanced Planarity

- **Copper Planarity**
  - D100 dramatically enhances bulk Cu planarization efficiency
  - D100 delivers improved dishing and erosion performance
Impact of Wettability on Low-K Rate

Low k Rate Control for Rs Variability Reduction

Second Generation Barrier

First Generation Barrier

Tailored Inhibitor Package

Selective Inhibitor

Dual Inhibitor System (BD-1 Specific)

Contact Angle

No Inhibitor

Low k RR (A/min)
Low K Removal Mechanism

Oxide (hydrolyzed) Incorporated
Black Diamond Surface

RR (hybrid) > or = RR (TEOS)

Black Diamond
(k= 2.7-2.8)

Surfactant
(BD Inhibitor)

Carbon Rich BD Surface
(More Hydrophobic)
Verification of Mechanism

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Tailored System Shows Enhanced Rs

Tailored system wafers have lower SD than control slurry ~ **49% improvement.**

Customer Validation of Rs Variability Reduction

**Overpolish Sensitivity**
Drawback of Passivation Chemistry

Suppression of Copper Rate

Results

Erosion: 44.55 nm
Dishing: 17.09 nm

Copper Protrusion

Requires Copper Rate Tunability
Copper Rate Control Mechanisms

- **Film Formation Control—Rate Suppression.**
  - Inhibitor Level—BTA for example.
  - Oxidizer Level—Peroxide for example.
- **Promotion Chemistry.**
  - Complexing Agent.
    - Structural Control.

Validation of Robust Film

- Enhanced Protection of Copper
- Complexer + BTA
- Complexer + BTA + Gen 2 Package
- Chosen Complexer

Increasing Hydrophobicity of Cu Complexing Agent

Yellow chosen based on balance between Film Formation and Removal
Increased “Chemical” Cu Rate Reduces Protrusion

Data Shown for Model S

Copper Dishing

Results

Erosion: 27.16 nm
Dishing: 2.90 nm

Latest Performance Shows Dishing < 100 Å, Erosion < 100 Å.
New CMP Applications In FEOL

- **Strain Engineering**
  - eSiGe, SiC, Si$_3$N$_4$
  - Selective and non-selective CMP steps

- **Replacement Metal Gate**
  - **New Dielectric**
    - Poly/Ox/Nit non-selective
    - Ox and/or Nit stop on Poly
  - **Metal Damascene**
    - Metal Silicidies (NiSi, CoSi, YbSi, etc.)
    - Al, TaCN, Ru

- **New Transistor Structures**
  - **New Dielectric**
    - Nit stop on OX, Nit/Ox non-selective

- **Si Replacement**
  - Ge, III/IV (InSb), InGaAs
New CMP Applications In BEOL

Alternative Liner CMP
- Ru, CuMn

Dielectric Cap
- Carbides, Nitrides

New Dielectric CMP
- Porous Low-k
- Air Gap
- Low Stress CMP?

Metal wire CMP Other than Cu?
- Al?

New Contact Metal CMP
- Cu, Rh
Additional New IC Related CMP Applications

- **DRAM**
  - New capacitor materials: Ru, TiN, Noble Metal?
  - Advanced poly CMP with high planarity

- **FLASH**
  - “Reverse” Poly for floating gate

- **New Non-Volatile Memory**
  - PRAM (GST CMP)
  - FeRAM (Noble Metal)

- **3D IC’s**
  - Through Si Vias
  - Thinning
Emerging Dielectrics and Exotic Materials

Other FEOL Dielectrics

Nitride/Oxide Selective

Colloidal Silica and Ceria Platforms

Nitride/Oxide Non selective

SiC

GST

Ru

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Emerging Metals and Exotic Materials

Noble Metals

Treated Alumina Platforms

Al

Ru
Developing Finishing Solutions for Multiple Applications

- Prime Silicon Wafer
- Flat Panel Displays
- Precision Optics
- Compound Semiconductor
- Healthcare
- Defense/Aerospace
- Solar Energy
- Data Storage/Hard Disk Drive
1. Unique complexer stabilizing H2O2 for consistent removal rates

2. > 10 mg/min removal rate over pad life for greater throughput with 7-9 nm size particles

3. ~1Å surface roughness (AFM Rₐ)

4. Less scratch severity
ESF Opportunities - Examples

**Aluminum Mirror Polishing**
Producing the best aluminum mirrors

**Single Point Diamond Turning**
- Grating effect due to turning marks
- Limited to > 50A rms
- Use limited to narrow frequency range

**ESF Polishing process**
- No grating effect
- Achieve < 15A rms
- Enable use in wide frequency range

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**Silicon Carbide Polishing**
Enabling higher rate

**ESF Gen I - commercialized**
- 2 X rate vs. POR
- Achieve 1 A rms reliably

**ESF Gen II – In development**
- 10 X rate vs. POR
- Achieve 1 A rms reliably

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Growing number of CMP applications drives strong need for consumables innovation

Innovation being achieved to support IC needs

Technology being extended outside of IC’s
Perfecting the Surfaces of Tomorrow™