Outline

❖ The Window
❖ The Results
  ✦ Magic Triangles
  ✦ Scratch That Itch
  ✦ Flipper
❖ The New, In With
❖ The End
The Window

Annual Wafer Starts (200mm equivalent)

Window of Opportunity

Source: Techcet Group, April 2011
The Window

✧ Fabs in a Downturn
  ✧ Clean, train, maintain
  ✧ Develop new ways to reduce cost
  ✧ Evaluate new products & methods

✧ Cost reduction impacts incumbents

✧ Evaluation time benefits insurgents

✧ Bonus motivation: customer dissatisfaction with current supplier
**Magic Triangles**

**Why now?**
- Years of talk about synergy between pad and slurry development produced *nothing*
- Crazy tight specs made us look more closely

**Systematic engineering work**
- Designed experiments
- New products available for evaluation
- Fab tool time available
- Fab engineer work product, no R&D transfer
Magic Triangles

- **Process characteristics**
  - Less aggressive pad conditioning
  - Highly reproducible pad roughness
  - Tight slurry PSD

- **Resulting observations**
  - Sharp reduction in surface scratches
  - Dishing meets aggressive specs
  - Exceptional removal rate stability
  - Lower CoO (pad life, conditioner life)
Magic Triangles

- Specific examples: CONFIDENTIAL
  - Patriot Act does not apply
  - Enhanced interrogation techniques off limits
    - Slurry-boarding on hold

- Magic triangle citations
  - Cabot (pads)
  - Fujimi
  - Hitachi
  - innoPad
  - Intel
  - Morgan
**Scratch That Itch**

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### Table FEP14  Shallow Trench Isolation CMP Process Technology Requirements

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM ½ Pitch (nm) (contacted)</td>
<td>52</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
<td>28</td>
</tr>
<tr>
<td>MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)</td>
<td>54</td>
<td>45</td>
<td>38</td>
<td>32</td>
<td>27</td>
<td>24</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>29</td>
<td>27</td>
<td>24</td>
<td>22</td>
<td>20</td>
<td>18</td>
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<tr>
<td>Wafer diameter (mm)</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>450</td>
</tr>
<tr>
<td>Wafer edge exclusion (mm)</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
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</table>

**Scratches**

<table>
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<tr>
<th></th>
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<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>Critical scratch length, $s_c$ (nm) [Å]</td>
<td>25.8</td>
<td>22.5</td>
<td>20.0</td>
<td>17.9</td>
<td>15.9</td>
<td>14.2</td>
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<tr>
<td>Critical scratch count, $S_{pw}$ (#/wafer) [Å]</td>
<td>40.1</td>
<td>40.1</td>
<td>40.1</td>
<td>40.1</td>
<td>40.1</td>
<td>166.3</td>
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**Uniformity**

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<th>2012</th>
<th>2013</th>
<th>2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMP total uniformity ($3\sigma$) for removal (%) [Å]</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>CMP uniformity ($3\sigma$) within wafer (%) [Å]</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
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<td>6</td>
</tr>
</tbody>
</table>

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[*Magic triangles will contribute to success*]

[*Critical scratch length <20nm, <40/wafer*]

Source: 2010 Interconnect ITRS

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Flipper

- **Old way**
  - Conditioner wears out, throw it away

- **New way**
  - Conditioner wears out, turn it over

- **Saint-Gobain introduces Flipper**
  - Abrasive on both sides
  - Reported CoO benefits 2.0x–2.5x
In With the New

Source: P. Feeney, Solid State Technology, November 2010

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In With the New

- Number of unique new CMP processes today is equivalent to total of all CMP steps at 0.25µm node
  - Single step R&D cost same as multi-step interconnect process
  - Unique by device type; few common to all

- Recession rewards
  - New collaborations, new personal relationships
  - Startups gain traction and momentum
The End

・ Both CMP users and suppliers will benefit from work completed during the recession

**Outlook from Semicon West 2010:**

・ CMP recovery is ahead of expectations
  ✷ CMP consumables revenue will surpass 2007 peak levels in 2010
  ✷ No residual impact beyond 2010

・ Market Update at Semicon West 2011
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