New CMP Applications
And Opportunities for Improvement

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Outline

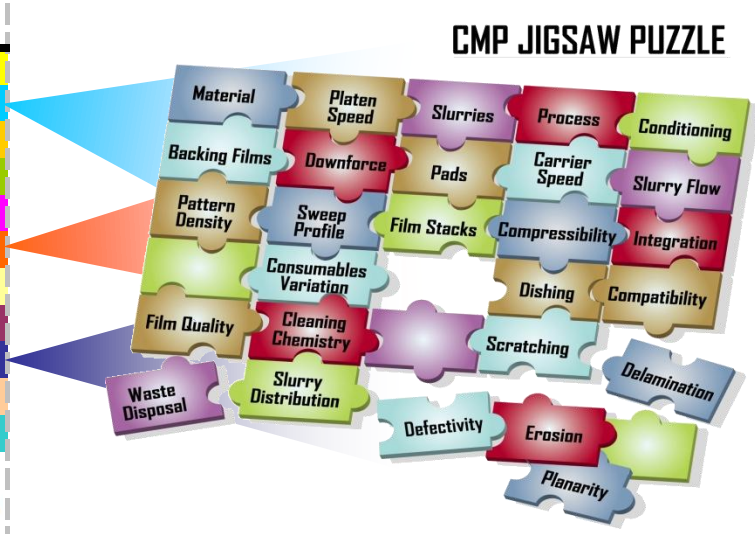
- Background
- TSV's
- Diamond CMP
- Opportunities for Improvement
- Summary

Background

- A trademark of the semiconductor industry is the relentless drive toward better, faster, & cheaper everything
- CMP became established as a mainstream CMOS process for oxide, tungsten, STI and copper planarization
- Numerous other technologies are now adapting CMP for new materials, different types of devices, etc.
  - Packaging
  - MEMS and Microfluidics
  - Novel substrates
  - Nanotechnology
  - Optics
  - Etc.

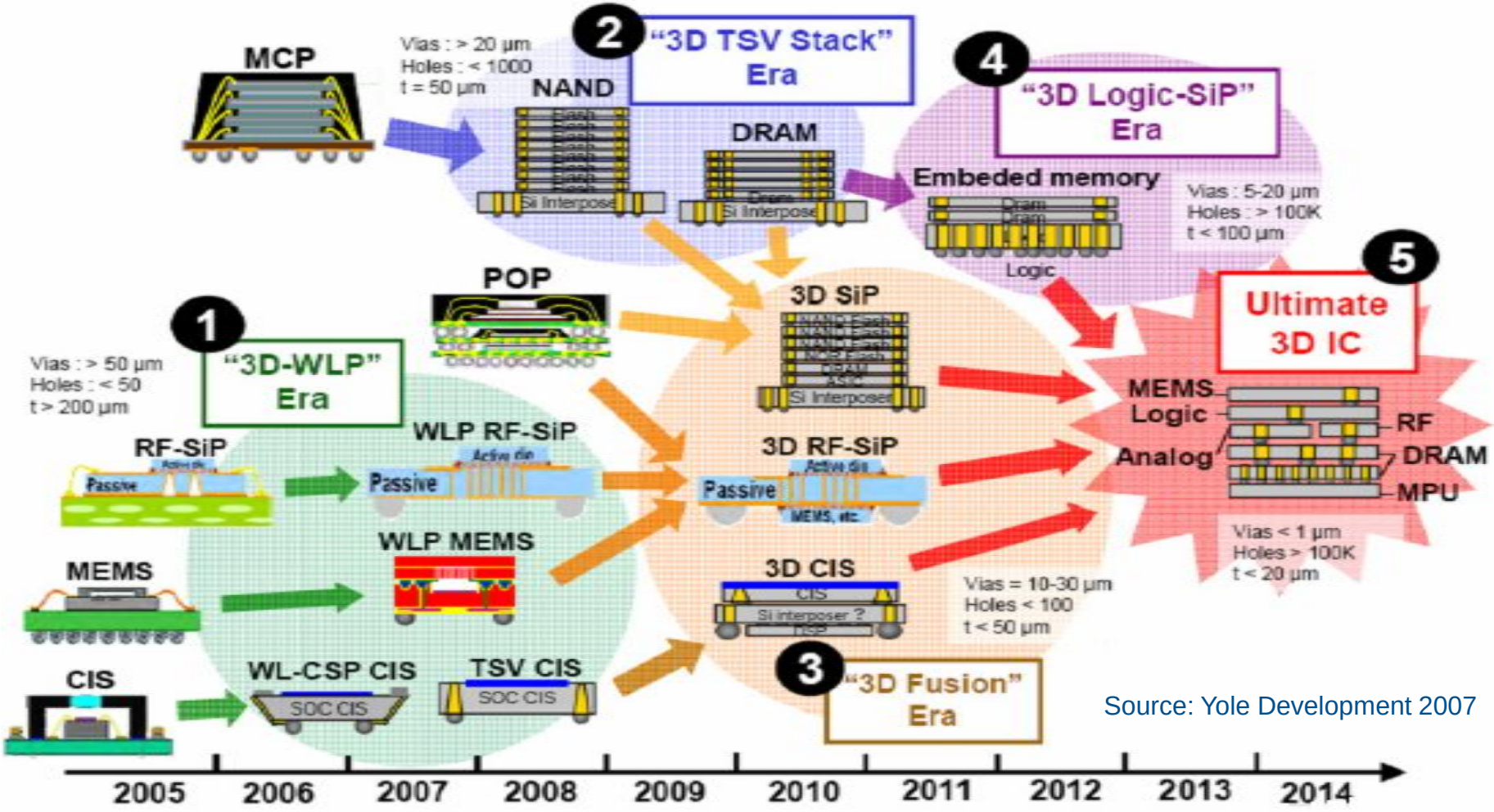
CMP Applications

1995 - Qty ≤ 2	2001 - Qty ≤ 5	2009 - Qty ≥ 36		
CMOS	CMOS	CMOS	New Apps	Substrate/Epi
Glass (oxide)	Glass (oxide)	Glass (oxide)	Doped Oxides	GaAs
Tungsten	Tungsten	Tungsten	Nitrides	GaN
	Copper	Copper	NiFe & NiFeCo	InP
	Shallow Trench	Shallow Trench	Noble Metals	CdTe & HgCdTe
	Polysilicon	Polysilicon	Al & Stainless	Ge and SiGe
		Low k	Polymers	SiC
		Cap Ultra Low k	Ultra Thin Wafers	Diamond & DLC
		Metal Gates	Direct Wafer Bond	Si & Reclaim
		Gate Insulators	Through Si Vias	SOI
		High k Dielectrics	3-D Packaging	Quartz
		Ir & Pt Electrodes	MEMS	Titanium
		Magnetics	Nanodevices	
			Integrated Optics	



As CMP applications continue to multiply … optimized consumables, processes and methods must be developed with lowest possible risk and cost

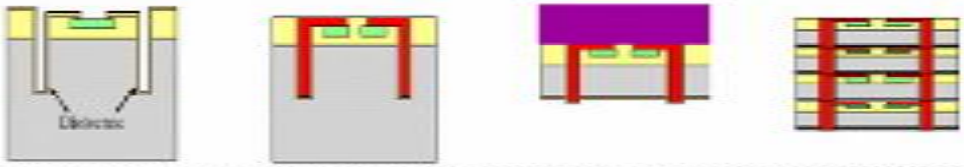
3D Packaging Apps



Source: Yole Development 2007

3D Scenerios

Scenario 1: Via drilling → Via filling → Thinning → Bonding



Fraunhofer, All-via, IMEC, ASET, Tohoku

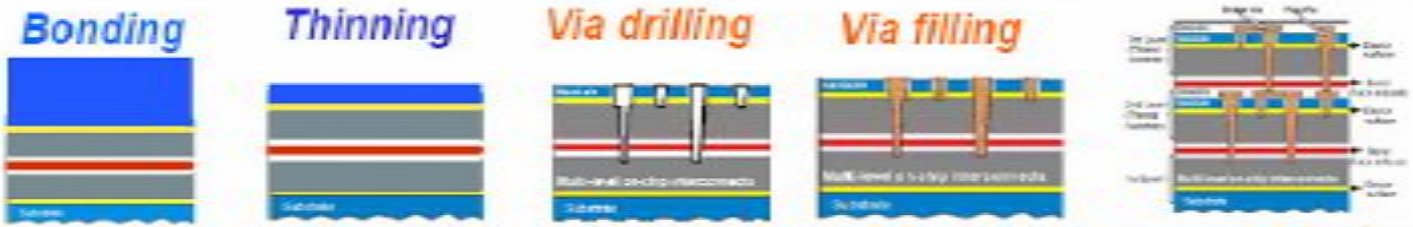
Scenario 2: Via drilling → Via filling → Bonding → Thinning

Tezzaron

Scenario 3: Thinning → Via drilling → Via filling → Bonding

Infineon

Scenario 4: Bonding → Thinning → Via drilling → Via filling

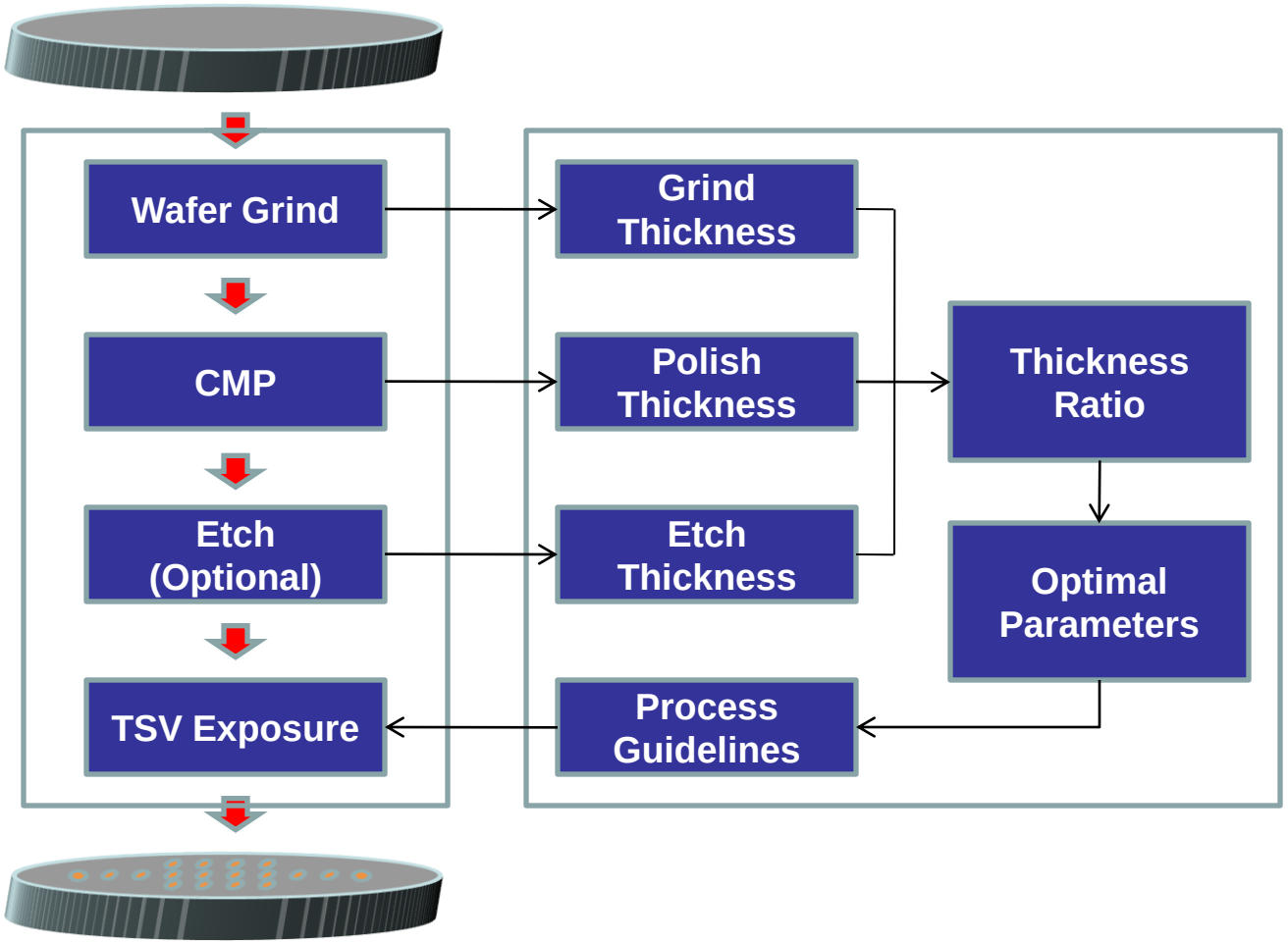


RPI

Packaging

- Vertical interconnects for 3D integration of electronics, MEMS, and other types of devices.
- CMP has been in development for advanced packaging for > 8 years.
- Deep vias can be filled with any of several conductive materials.
  - Most common options are copper and polysilicon.
  - Final choice depends on dimensions, operating voltage and current, frequency, plus other integration factors.
- Vias can be completely filled or left partially hollow
  - Hollow vias can be quite difficult to clean after CMP

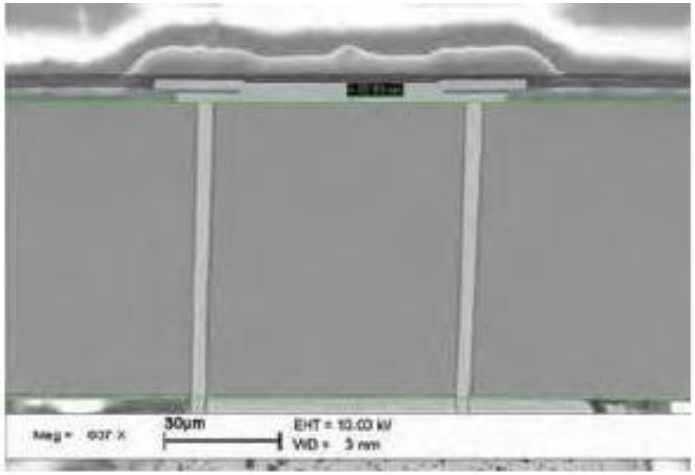
Typical TSV Flow



TSV Summary Table

TSV Fill Material	Deposition Thickness	Demonstrated CMP Polish Rate	Dishing / Recess (Angstroms)
Copper	5 kA – 60 µm	1 kA/min – 8 µm/min	10 A – 0.3 µm
Polysilicon	4 kA – 30 kA	2 kA/min – 15 kA/min	300 – 1200 Ang
Tungsten	3 kA – 9 kA	3 kA;/min – 8 kA/min	150 – 300 Ang
NiFe or NiFeCo	1.5 µm – 8 µm	3 kA/min – 7 kA/min	600 – 4000 Ang
Pt	1.5 µm – 5 µm	1.5 kA/min – 5 kA/min	100 – 800 Ang

Copper Vias



Source: IBM

- Numerous customers are using plated copper for TSV's
- Typical via sizes 5–100 µm and plating thicknesses 3–40 um
- Cu recess below 0.4 um achieved for multiple trials
- Characterized CMP interactions with cumulative film stress, wafer shape, annealing, etc.

2nd Example: Cu (stop on TEOS)

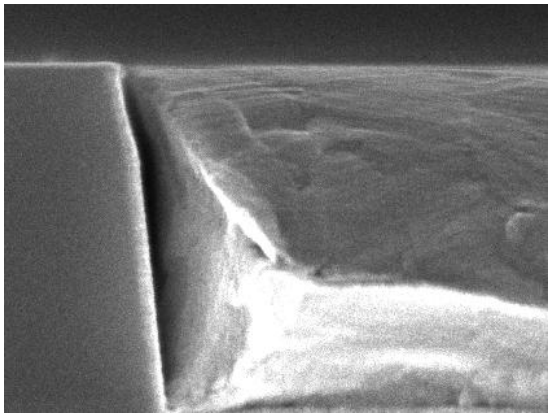
- Intended integration = Direct Wafer Bonding
- Goal of <200 A total topography

POST-CMP TOPOGRAPHY ACHIEVED

70-90 Angstroms

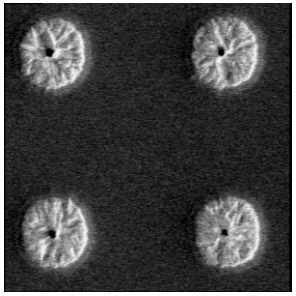
→

Flat across Feature

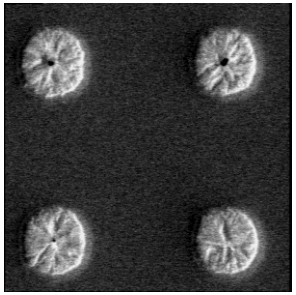


Tungsten Vias

- Technology adapted from proven CMOS device integrations
- Typical via sizes are sub-micron but many vias can be ganged in parallel for higher current
- Typical W recess achieved is below 500 Ang
- Relatively mature CMP approach, but integration can be difficult, esp. stress control



Center



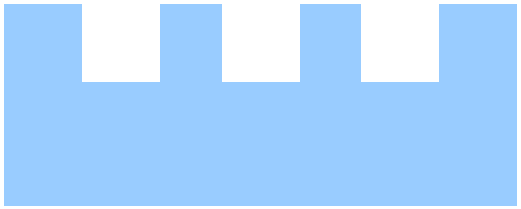
Edge

Pt Vias

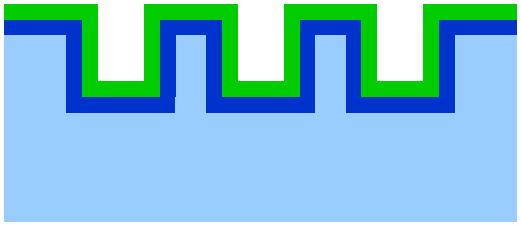
- Some devices require high temperature processes, such as annealing of piezoelectric layers
  - RF switches, cantilever sensors, and acoustic transducers
- Fabricating TSV's prior to MEMS (via-first approach) requires materials that can withstand high annealing temperatures needed for piezoelectric films (>600^{o}C)
- Platinum is a potential candidate, but fabrication techniques for Pt vias are not yet mature

Process Flow (partial)

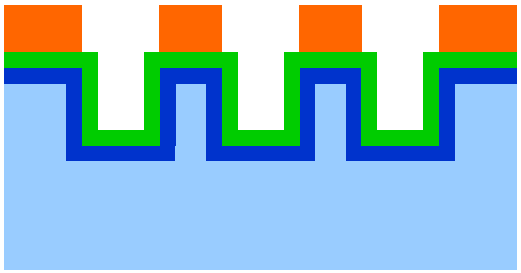
1. Etch vias in SOI substrate
   3-7 μm dia.
   5 μm depth



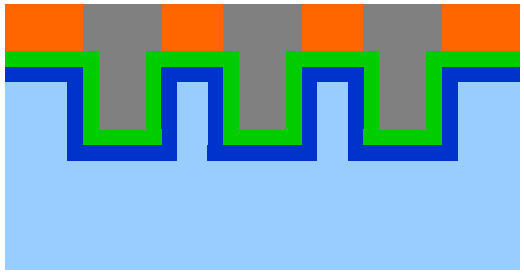
2. Oxidize silicon
   (1 μm); sputter Ti/Pt seed
   (0.7 μm)



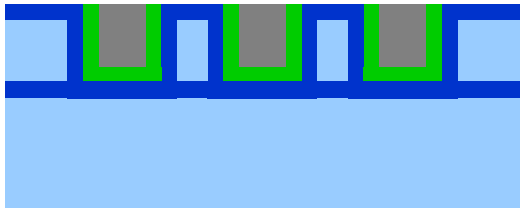
3. Deposit resist plating template
   (3.5 μm)



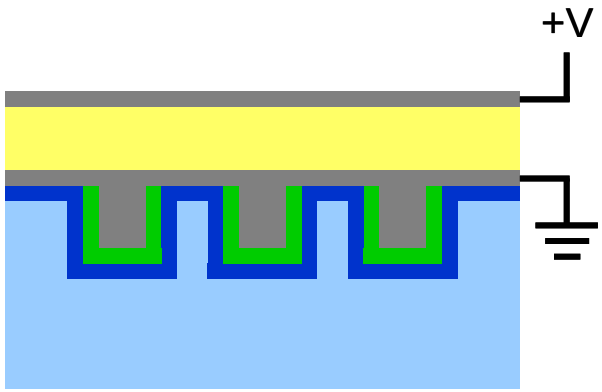
4. Plate Pt to fill vias; remove resist



5. CMP Pt over-burden, stopping on SiO_2

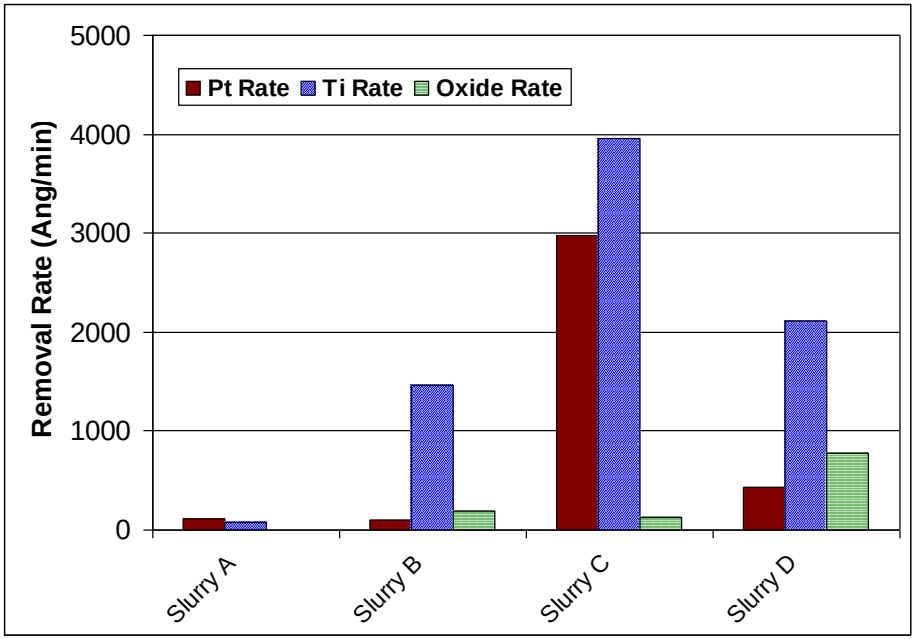


6. Evaporate electrodes, spin coat PZT (1μm), anneal
   (700°C)



CMP Slurry Screening

- CMP screening experiments to determine removal rates
- Process targets:
  - Pt (RR > 2000 Ang/min)
  - Ti (RR > 2000 Ang/min)
  - SiO_2 (High selectivity)
  - Good surface quality
- Slurry C met required performance and was used for further work

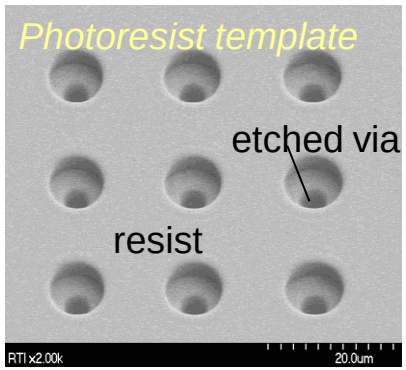


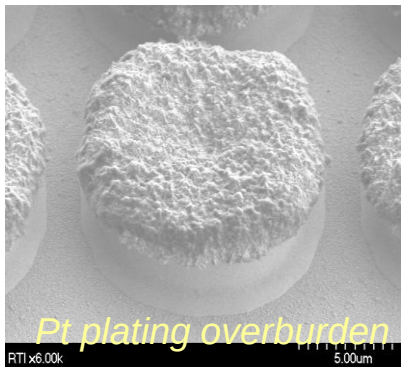
Slurry	Pt Rate (A/min)	Ti Rate (A/min)	Tox Rate (A/min)	Selectivity (Pt:Ti)	Selectivity (Ti:Oxide)
A	12	8	<1	1.5	> 8
B	104	1461	195	0.1	7.5
C	2980	3955	132	0.8	30.0
D	436	2108	777	0.2	2.7

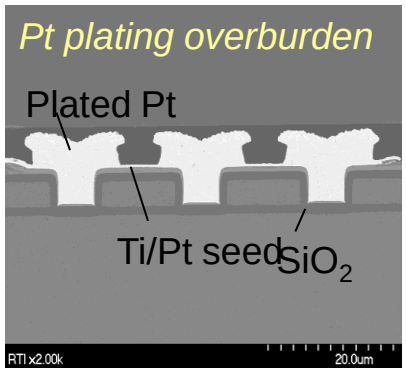
Pt Vias

- Electroplated Pt for via fill
- Tolerates high temperatures up to 700°C

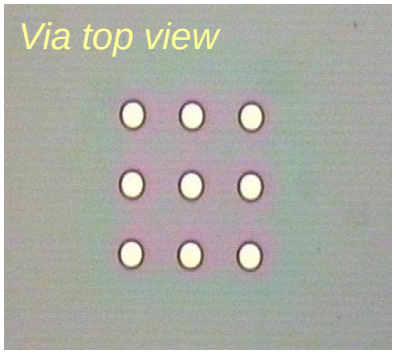
Pre-CMP

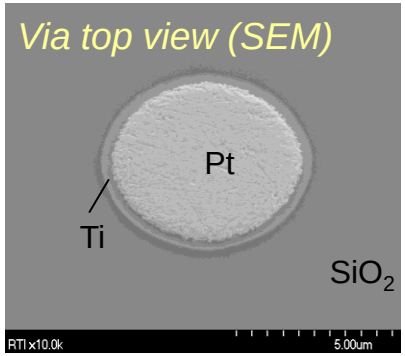


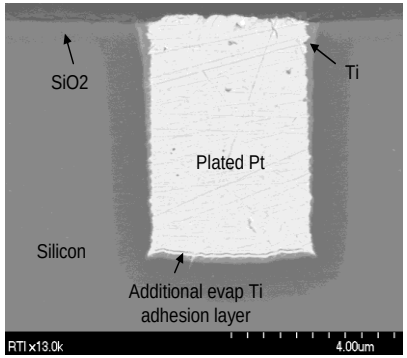




Post-CMP







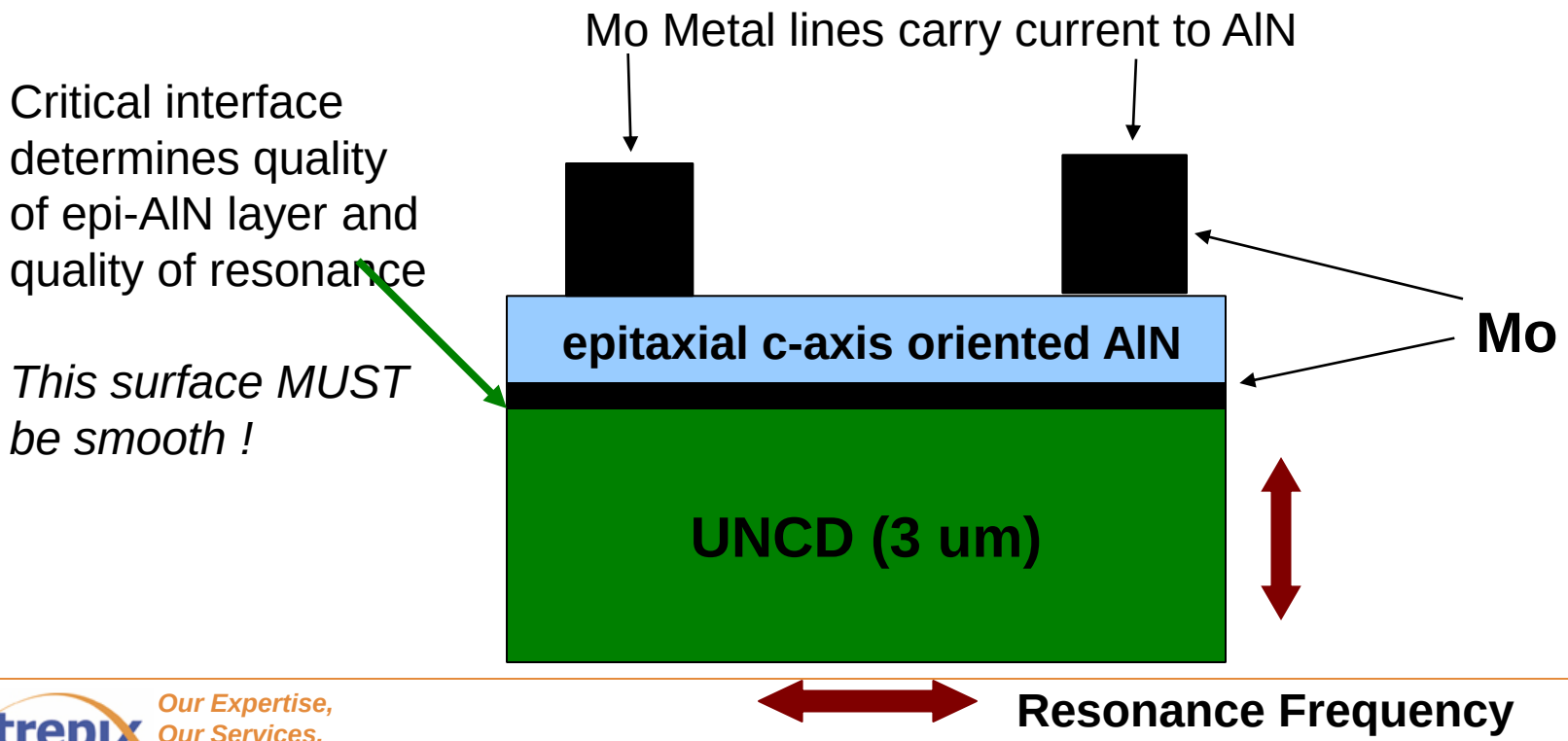
Diamond CMP

- Polycrystalline diamond films
  - Extremely hard and chemically inert
  - Optimized deposition/growth to improve starting Ra
  - Still slightly rough as deposited (Ra ~10 nm)
- Desired process targets
  - Roughness < 1 nm (Ra on 3 x 3um AFM)
  - Total removal < 100 nm (prefer < 50 nm)
  - Scratch-free and particle-free final surfaces
- Example application = RF MEMS Oscillator

Simplified Schematic

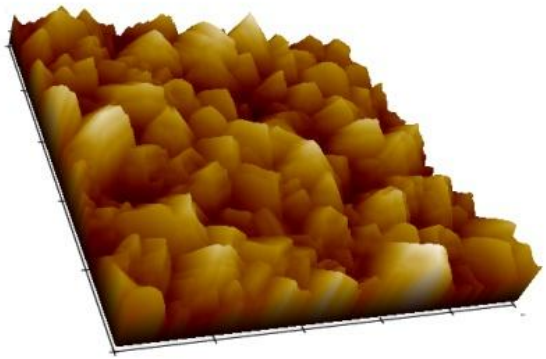
• UNCD resonates with frequency dependent upon its Young's Modulus and film thickness. Diamond has the highest acoustic velocity and YM of any material.

• Piezoelectric signal imparted by high efficiency piezoelectric material (AlN)



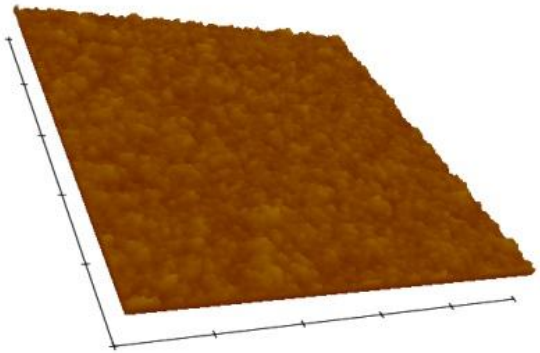
Diamond Surfaces

Roughness > 50 nm RMS



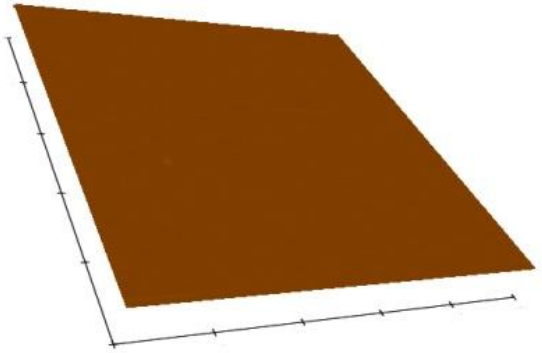
Typical deposition

Roughness = 10 nm RMS



Optimized deposition

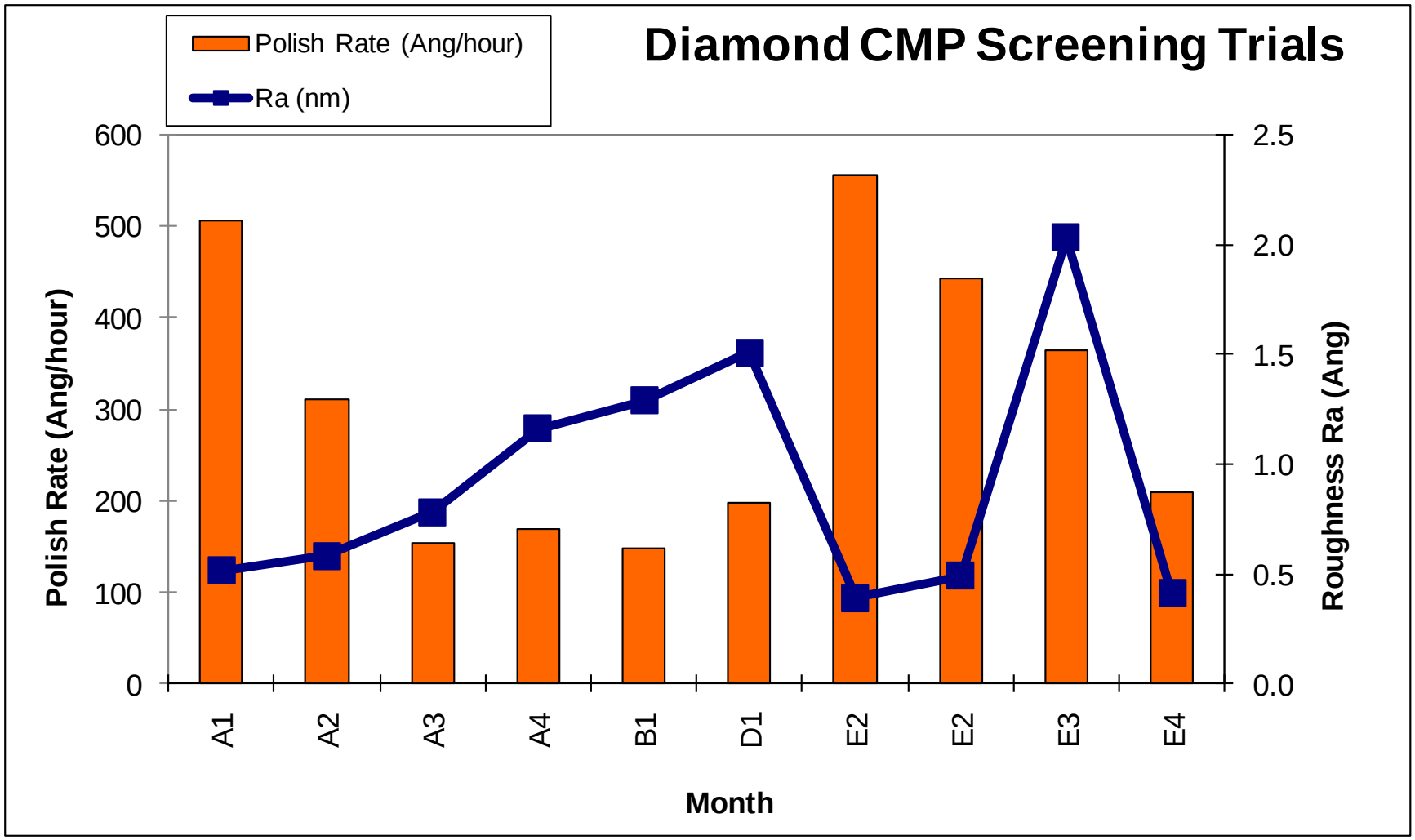
Roughness < 1 nm RMS



After CMP

All images taken by AFM using 5x5 um field of view and same vertical scale

Screening Trials



Effect on Devices

Effect of UNCD Roughness on Crystal Quality of Piezoelectric AlN Layer (X-ray Rocking Curve FWHM)

3.0 um UNCD

Wafer ID	Intrinsic AlN Film Stress (MPa)	Mo Rocking Curve FWHM	AlN Rocking Curve FWHM	Comment
3702	-131	6.3º	5.7º	CMP polished to less than 1nm RMS
4350	+5	5.8º	5.0º	CMP polished to less than 1nm RMS
6228	-164	>11º	>12º	As-deposited Aqua25 UNCD (6-8 nm RMS)
6229	-80	10.5º	11.2º	As-deposited Aqua25 UNCD (6-8 nm RMS)

Improvements

- **Performance**
  - Often drives the initial development effort
  - CMP process MUST meet minimum requirements which are very different between applications and nodes
- **Repeatability**
  - Often becomes a most critical factor in manufacturing
  - Can be tough to troubleshoot (numerous sources)
  - Most process engineers will trade a bit of extra performance to improve consistency … in a heartbeat!
- **Cost**
  - Increasingly driving decisions
  - No longer focused on simply consumables

CMP Performance

- Wafer Level Metrics
  - Removal Rates and Selectivities
  - Uniformity
  - Planarization (roughness,dishing,erosion,etc.)
  - Defectivity
- Integration drives CMP requirements
- Device design drives integration
- Market drives device design (& cost targets)
- Performance gaps can appear at any time
  - New products or evolution in existing markets

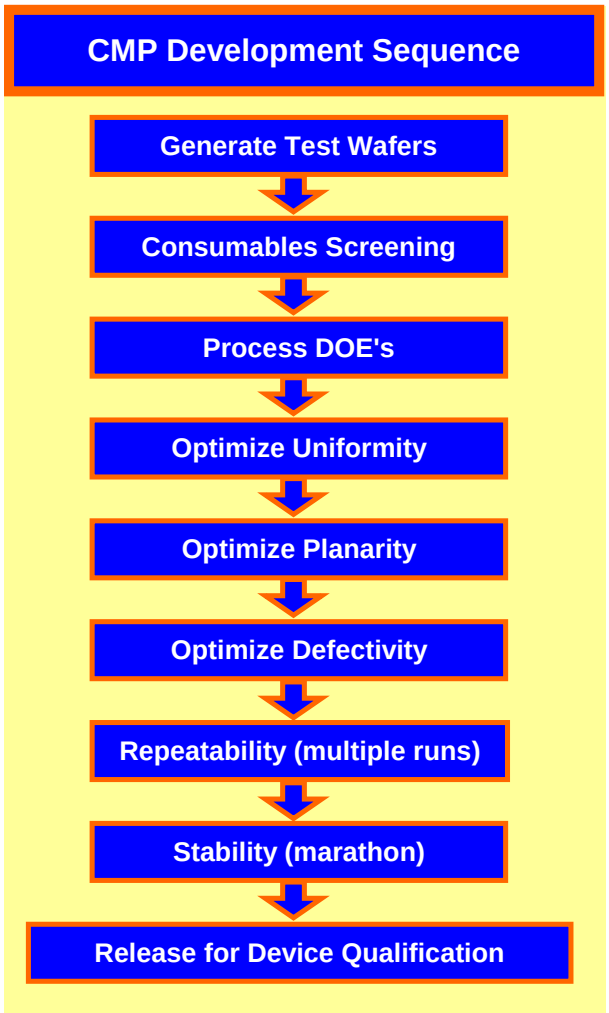
Early CMP Stages

Early stage development efforts often involve:

- Immature deposition or growth processes
- Poorly characterized materials or integrations
- Technologists who may not be familiar with CMP and how it interacts with other process modules
- Wide variation in pattern density/feature sizes
- Wafer sizes smaller than 200 mm
- Limited availability of test wafers

These factors can create huge challenges for CMP

CMP Development



- Zoom in on CMP process development
- Experience with broad range of materials, pads, and slurries is key to efficiency
- Test wafer availability and quality often impact timeline, validity of results, etc.
- Initial process DOE's generally focus on removal rate and surface quality
- Optimization stages can be interchanged or executed in parallel
- Planarity can mean step height, dishing, recess, roughness, etc. depending on the material and intended application
- Metrics are specific to each integration and can be adjusted as required

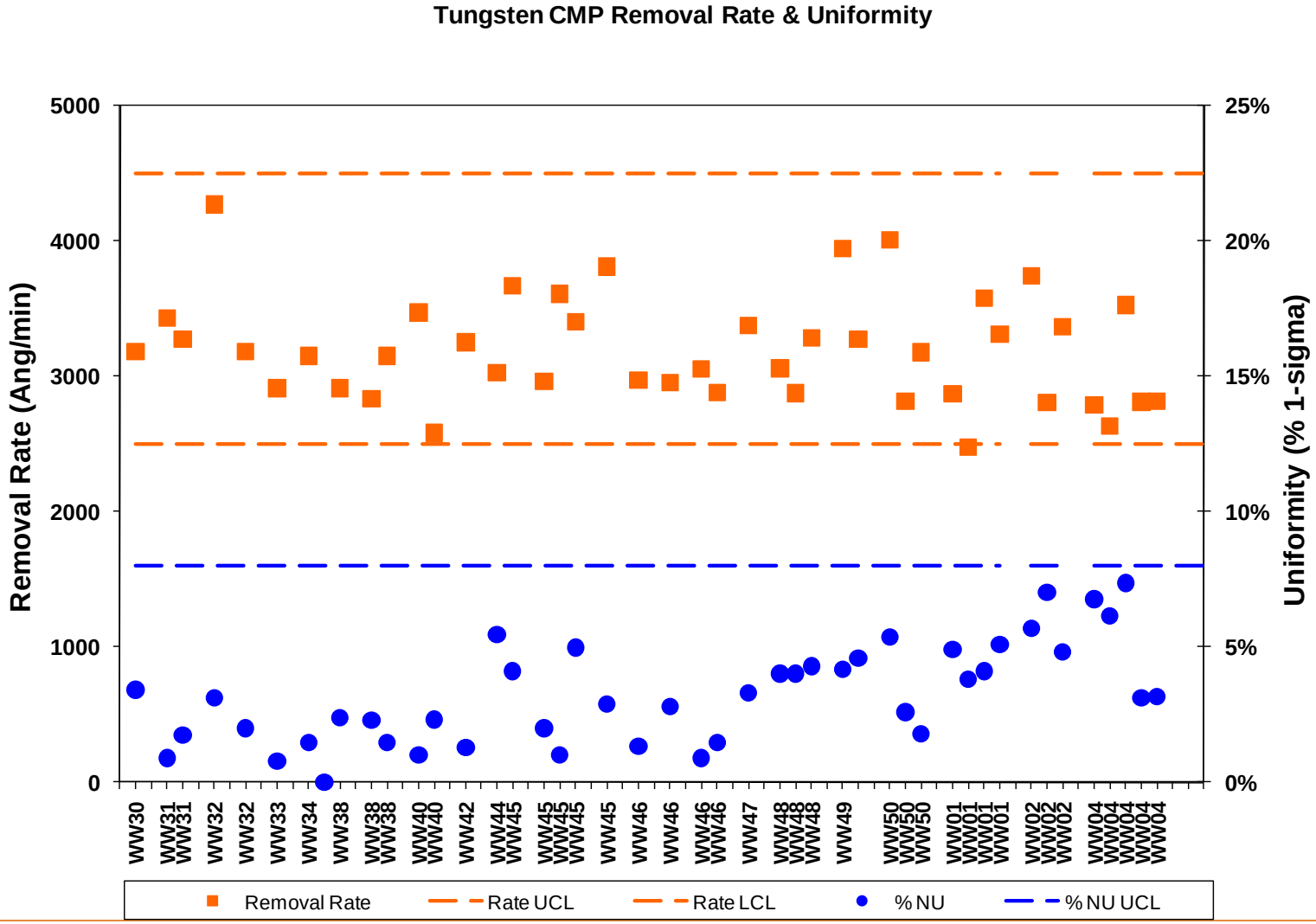
CMP Complexity

- **Wafer / Materials Parameters**
  - Size / Shape / Flatness
  - Film Stack Composition
    - Metals (Al, Cu, W, Pt, etc.)
    - Oxide (TEOS, PSG, BPSG, etc.)
    - Other (polysilicon, low-k polymers, etc.)
  - Film Quality Issues
    - Stress (compressive or tensile)
    - Inclusions and other defects
    - Doping or contaminant levels
  - Final Surface Requirements
    - Ultralow surface roughness
    - Extreme planarization, esp. Copper
    - Low defectivity at <0.12 um defect size
- **Pad Issues**
  - Materials (polyurethane, felt, foam, etc.)
  - Properties must be chosen for the job
  - Conditioning method often not optimized
  - Lot-to-lot consistency
- **Slurry Issues**
  - Chemistry optimization often required
  - Mixing and associated inconsistency
  - Shelf life and pot life sometimes very short
  - Slurry distribution system (design, cost, upkeep)
    - Agglomeration and gel formation
    - Filtration is often required
  - Cleaning method specific to slurry and film
  - Waste disposal and local regulations

- **Process Issues**
  - Long list of significant input variables
    - Downforce
    - Platen speed
    - Carrier speed
    - Slurry flow
    - Conditioning method
      - Disk used (material, diamond size, spacing, etc)
      - Force
      - Speed
      - Sweep profile
  - Highly sensitive to local pattern variation
  - Must maintain consistency at high throughput
  - Must optimize for variation of incoming films
- **Integration Issues**
  - Materials Compatibility
    - Electrochemical interactions with two or more metals
    - Film integrity and delamination, esp. low-k
    - Film stack compressibility
  - Interactions with adjacent process modules
    - Photolithography
    - Metal deposition and metal etch
    - Dielectric deposition and etch
  - Electrical design interactions
    - Feature size constraints
    - Interactions with local pattern density
    - Line resistance variation, esp. damascene copper
    - Dielectric thickness variation
    - Contact resistance variation

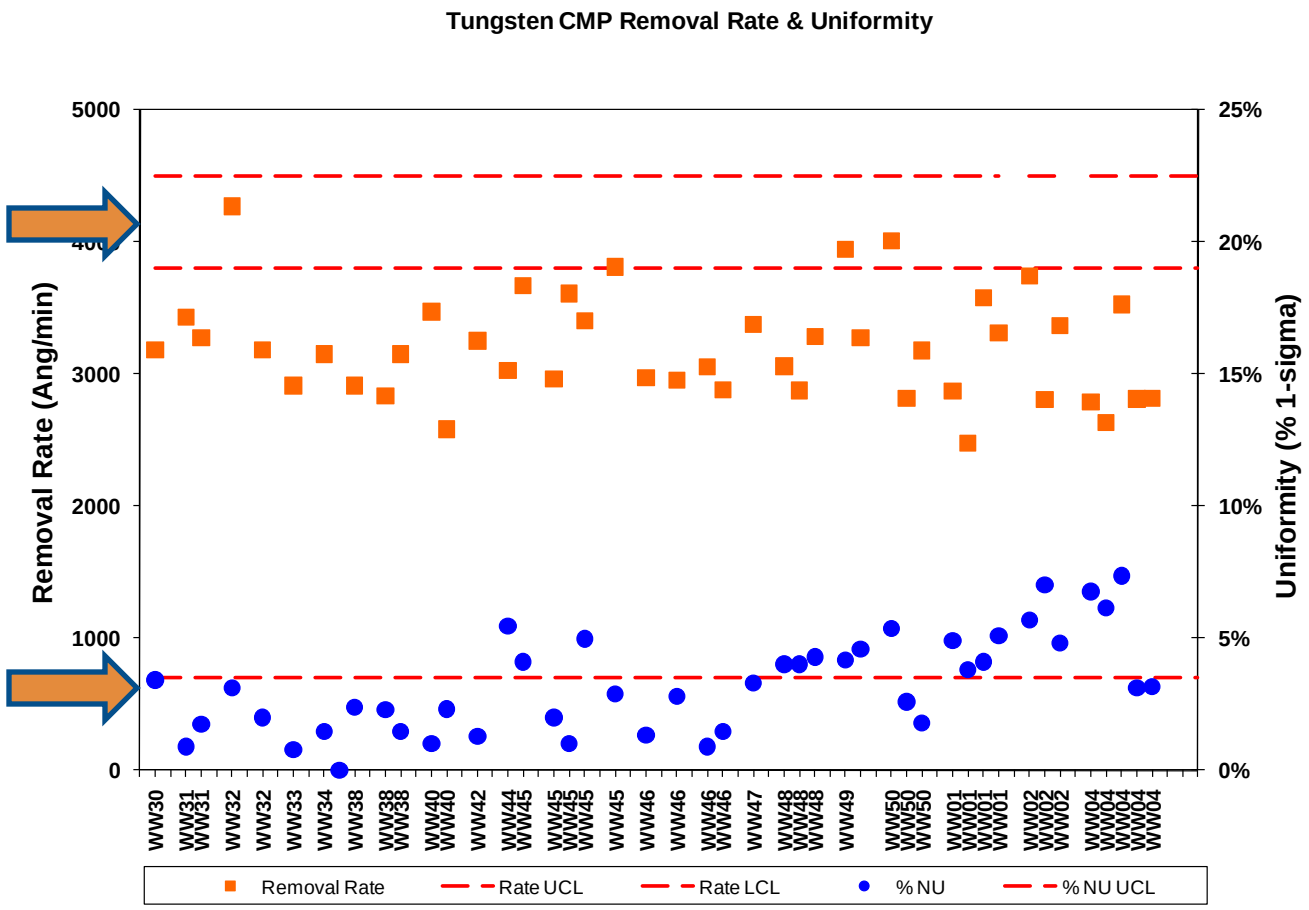
Many of these influence both performance & repeatability

Past Repeatability



Repeatability Goals

- Requirements often get tighter with next generation devices
- Option 1: Redevelop process to tighten variation
- Option 2: Find ways to tolerate variation
  - Endpoint
  - Integration



Sources of Variation

- Familiar Sources
  - Slurry (pH, particles, etc.)
  - Pads
  - Conditioning disks
  - Wear during pad life
  - Test wafer vs product wafer

- Less obvious
  - Contamination
  - Distribution system
  - Pumps & filters
  - Slurry dispense location
  - Source of H2O2
  - Head rebuild technique
  - DI water temperature
  - Metrology instability (Are you chasing a ghost?)
  - Bake/anneal sensitivity
  - Barrier metal grain structure
  - Pattern density / layout

Cost Introduction

- In early years, CMP was forgiven for being an expensive process because it enabled entire generations of devices
- Economic reality is now driving cost reduction efforts
- Costs can be generally divided into 3 categories
  - Development costs
  - Capital
  - Operating (per wafer pass)

Development Costs

- Classic engineering tradeoff: Speed, Low Cost, or Quality (choose 2)
- Shorter product life means shorter timeline for next gen
- Development $$ have to be amortized over product life

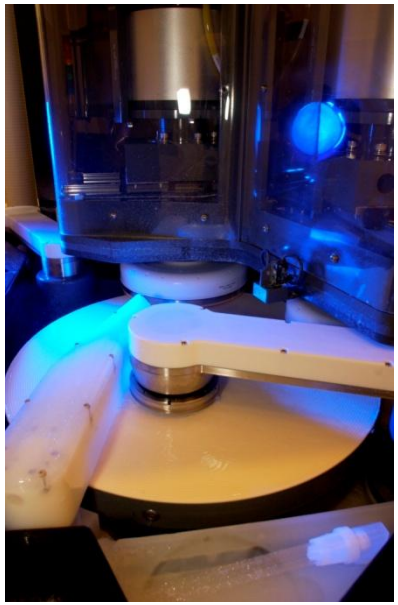
Actions being taken by fabs to control development costs:

- Extreme prioritization and focus (no “science projects”)
- Push early screening and optimization down to suppliers
- Outsource non-critical functions or bring in outside resources
- Alliances and consortia to share next gen development costs

Development Costs

- Ways to reduce CMP development costs
  - Avoid it (extend existing process if possible)
  - Get someone else to pay for it
  - Get someone else to at least share the cost
  - Talk to suppliers and leverage their experience
  - Engage outside resources with expertise
  - Be efficient … Follow a disciplined approach
  - Literature search (web surfing is cheap)

Capital Costs

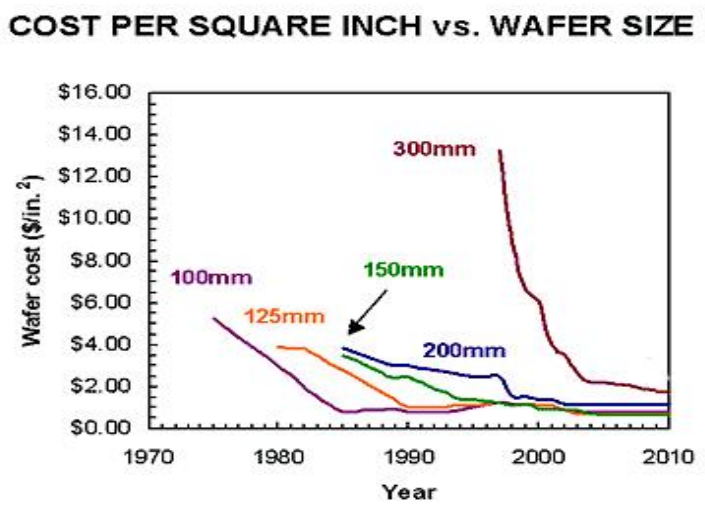


- Leading edge fabs still spend huge $$$ on WFE
- Older fabs being extended well beyond original design life or being repurposed to other devices
- Pricing factors for new tools depend on the OEM

Actions being taken by fabs to control capital costs:

- Increasingly popular “fab lite” model (or outsource altogether)
- Extend installed base whenever possible (may include upgrades)
- Repurpose or sell certain fabs
- Some choosing to buy refurbished rather than new tools

Operating Costs



- Consumables are an obvious target for cost savings
- Competition among providers enhances price erosion in some markets (e.g. Cu stock slurries)
- Supplier margins being squeezed

Actions being taken by fabs to control operating costs:

- Maximize throughput & minimize CMP polish times (integration)
- Increase slurry dilution and run lowest flow possible
- Extend pad life, especially with optimized conditioning
- Apply price pressure on suppliers (cost alone can justify switch)

CMP: New Definition

- Competitive pressures are increasing in most device markets over time
- Long-term viability for device manufacturers depends on controlling costs at all levels

CMP = Cost Managed Processes

Summary

- Through Silicon Via Technology (TSV)
  - Options for conductive materials: Cu, W, Pt, polysilicon, etc.
  - Wafer level requirements typically different than CMOS
    - More demanding for rate/throughput, less demanding for dishing/erosion
- Diamond CMP
  - Extremely hard and inert material
  - Roughness below 1nm has been achieved with CMP
  - Demonstrated improvement in RF resonance
- Opportunities for CMP Improvement
  - Performance
  - Repeatability
  - Cost

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Consumer Drivers

- **Since 2005, consumer products have become primary industry driver.**
- **Short product life cycles.**
- **Consumers demand *More for Less*.**
- **Consumers demand *More in Less Space*.**
- **Historically enabled by Moore's Law – device shrinks & larger wafers.**
- **Result = Fierce Competition**

  + Control Unit Costs
  + Develop Technology Fast
  + Ramp Volume Quickly

Source: 2007 Industry Strategy Symposium – Hans Stork, CTO, Texas Instruments

Source: 2007 Industry Strategy Symposium – Steve Newberry, CEO, Lam Research Corporation